Listing of Claims:

This listing of claims replaces all prior versions and listing of claims in the application. Amendments or cancellations of any claims are done without prejudice, waiver and/or disclaimer. Assignee reserves the right to claim the subject matter of any amendment and/or cancellation in a continuing application:

1. (Currently Amended) A semiconductor device ~~suitable for applications in an electrostatic discharge (ESD) protection circuit~~, comprising:

a semiconductor substrate;

a first well formed in the substrate;

a second well formed in the substrate;

a first doped region formed in the second well,

a second doped region formed in both the first well and the second well; and

a deep well formed in the substrate that physically isolates the substrate from at least the second well,

wherein the first well, the second well, and the first doped region collectively form a parasitic bipolar junction transistor (BJT),

wherein the first well ~~is the~~ comprises a collector of the BJT, the second well ~~is the~~ comprises a base of the BJT, ~~and~~ the first doped region ~~is the~~ comprises an emitter of the BJT, and wherein the second doped region is adapted to receive a trigger current or a trigger voltage[[,]] ~~and~~

~~wherein the deep well does not form a terminal of a transistor~~.

2. (Currently Amended) The semiconductor device of claim 1, wherein the first well ~~is~~ comprises an n-type well, the second well ~~is~~ comprises a p-type well, the first doped region ~~is~~ comprises an n-type region, and the parasitic BJT ~~is~~ comprises an NPN BJT.

3. (Currently Amended) The semiconductor device of claim 1, wherein the first well ~~is~~ comprises a p-type well, the second well ~~is~~ comprises an n-type well, the first doped region ~~is~~ comprises a p-type region, and the parasitic BJT ~~is~~ comprises a PNP BJT.

4. (Currently Amended) The semiconductor device of claim 1, further comprising:

~~a second doped region formed in the first well; and~~

a third doped region formed in the substrate,

wherein the second doped region and the first well ~~are of~~ comprise a same type of conductivity, and the second doped region ~~is~~ comprises a contact to the first well, and

wherein the third doped region and the second well ~~are of~~ comprise a same type of conductivity, and the third doped region ~~is~~ comprises a contact to the second well.

5. (Currently Amended) The semiconductor device of claim 4, further comprising an ESD detection circuit,

wherein the first doped region is connectable to a power supply,

wherein the second doped region is connectable to a contact pad for receiving an ESD current, and

wherein the third doped region is connectable to the ESD detection circuit coupled to the contact pad for detecting the ESD current.

6. (Currently Amended) The semiconductor device of claim 5, wherein the ESD detection circuit ~~provides~~ is adapted to provide a trigger current to the third doped region in an ESD event, and

wherein in response to the trigger current ~~triggers~~ the parasitic BJT is adapted to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region.

7. (Currently Amended) The semiconductor device of claim 5, wherein the BJT ~~is~~ comprises an NPN BJT, and the power supply ~~is~~ comprises ground.

8. (Currently Amended) The semiconductor device of claim 5, wherein the BJT ~~is~~ comprises a PNP BJT, and the power supply ~~is~~ comprises a positive supply voltage.

9. (Currently Amended) The semiconductor device of claim 5, further comprising a fourth doped region formed in the second well,

wherein the fourth doped region and the second well ~~are of~~ comprise a same type of conductivity, wherein the fourth doped region ~~is also~~ comprises a contact to the second well, wherein the third doped region and the fourth doped region are spaced apart from each other, and wherein the fourth doped region is connectable to the power supply.

10. (Currently Amended) The semiconductor device of claim 1, further comprising

~~a second doped region formed in the first well;~~

a third doped region formed in the substrate; and

a fourth doped region formed in the second well,

wherein the first, second, third, and fourth doped regions are electrically isolated from each other by a plurality of isolation regions.

11. (Currently Amended) The semiconductor device of claim 10, wherein the isolation regions ~~are~~ comprise shallow trench isolations (STIs).

12. (Currently Amended) The semiconductor device of claim 10, wherein the isolation regions ~~are~~ comprise oxidation of silicon (LOGOS) regions.

13. (Currently Amended) The semiconductor device of claim 1, further comprising

~~a second doped region formed in the first well;~~

a third doped region formed in the substrate; and

a fourth doped region formed in the second well,

wherein the first, second, third, and fourth doped regions are electrically isolated from each other by a plurality of dummy gate structures.

14. (Original) The semiconductor device of claim 13, wherein the gates of the dummy gate structures are doped with both P^+ and N^+ dopants, wherein a portion of the gates proximate a p-type doped region is doped with P^+ dopant, and a portion of the gates proximate an n-type doped region is doped with N^+ dopant.

15. (Currently Amended) The semiconductor device of claim 1, ~~further comprising a second doped region for receiving a trigger current or a trigger voltage in an ESD event, wherein a portion of the second doped region is formed in the first well, and another portion of the second doped region is formed in the second well~~, and wherein in response to the trigger current or the trigger voltage ~~triggers~~ the BJT is adapted to discharge current ~~the ESD~~ in the ESD event.

16. (Currently Amended) A semiconductor device ~~suitable for applications in an electrostatic (ESD) protection circuit~~, comprising:

a semiconductor substrate;

a first well formed in the substrate;

a second well formed in the substrate;

a third well formed in the substrate; and

a first doped region formed in the second well,

wherein the first well, the second well, and the first doped region collectively form a first parasitic bipolar junction transistor (BJT), and wherein the second well, the third well, and the first doped region collectively form a second parasitic BJT, and wherein the first well ~~is the~~ comprises a collector of the first BJT, the third well ~~is the~~ comprises a collector of the second BJT, the second well ~~is the~~ comprises a base of both of the first and the second BJTs, and the first doped region ~~is the~~ comprises an emitter of both of the first and the second BJTs.

17. (Currently Amended) The semiconductor device of claim 16, wherein the first BJT and the second BJT ~~are both~~ comprise NPN-BJTs.

18. (Currently Amended) The semiconductor device of claim 16, wherein the first BJT and the second BJT ~~are both~~ comprise PNP BJTs.

19. (Currently Amended) The semiconductor device of claim 16, further comprising

a second doped region formed in the first well;

a third doped region formed in the third well;

a fourth doped region formed in the substrate; and

a fifth doped region formed in the substrate,

wherein the second doped region and the first well ~~are of~~ comprise a same type of conductivity, and the second doped region ~~is~~ comprises a contact to the first well,

wherein the third doped region and the third well ~~are of~~ comprise a same type of conductivity, and the third doped region ~~is~~ comprises a contact to the third well, and

wherein the fourth doped region, the fifth doped region, and the second well ~~are of~~ comprise a same type of conductivity, wherein the fourth doped region and the fifth doped region ~~are both~~ comprise contacts to the second well, and wherein the fourth doped region and the fifth doped region are spaced apart from each other.

20. (Currently Amended) The semiconductor device of claim 19,

wherein the first doped region is connectable to a power supply,

wherein the second and the third doped regions are connectable to a contact pad for receiving an ESD current, and

wherein the fourth and fifth doped regions are connectable to an ESD detection circuit, wherein the ESD detection circuit is coupled to the contact pad for detecting the ESD current.

21. (Currently Amended) The semiconductor device of claim 20, wherein the ESD detection circuit ~~provides~~ is adapted to provide a trigger current or a trigger voltage to the fourth and fifth doped regions in an ESD event, wherein in response to the trigger current or trigger voltage provided to the fourth

doped region ~~triggers~~ the first BJT is adapted to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region, and in response to the trigger current or trigger voltage provided to the fifth doped region triggers the second BJT is adapted to conduct the ESD current from the third doped region to the first doped region or from the first doped region to the third doped region.

22. (Original) The semiconductor device of claim 19, wherein the first, second, third, fourth, and fifth doped regions are electrically isolated from each other.

23. (Currently Amended) The semiconductor device of claim [[16]] 19, further comprising a plurality of dummy gate structures to electrically isolate at least two of the first, second, third, fourth, and fifth doped regions.

24. (Original) The semiconductor device of claim 23, wherein the gates of the dummy gate structures are doped with both P^+ and N^+ dopants, wherein a portion of the gates proximate a p-type doped region is doped with P^+ dopant, and a portion of the gates proximate an n-type doped is doped with N^+ dopant.

25. (Original) The semiconductor device of claim 19, wherein a portion of the fourth doped region is formed in the first well, and another portion of the fourth doped region is formed in the second well, and wherein a portion of the fifth doped region is formed in the second well, and another portion of the fifth doped region is formed in the third well.

26. (Currently Amended) A semiconductor device ~~suitable for applications in an electrostatic discharge (ESD) protection circuit~~, comprising:

a semiconductor substrate;

a first well formed in the substrate;

a second well formed in the substrate;

a third well formed in the substrate;

a deep well formed in the substrate that physically isolates the substrate from the first, second, and third wells:

a first doped region formed in the second well; ~~and~~

a second doped region formed in the second well,

a third doped region formed in both the first well and the second well;

a fourth doped region formed in the second well; and

a fifth doped region formed in both the second well and the third well,

wherein the first well, the second well, and the first doped region collectively form a first parasitic bipolar junction transistor (BJT), and the second well; the third well, and the second doped region collectively form a second parasitic BJT, and

wherein the first well ~~is the~~ comprises an emitter of the first BJT, the third well ~~is the~~ comprises an emitter of the second BJT, the second well ~~is the~~ comprises a base of both of the first and the second BJTs, the first doped region ~~is the~~ comprises a collector of the first BJT, and the second doped region ~~is the~~ comprises a collector of the second BJT.

27. (Currently Amended) The semiconductor device of claim 26, further comprising

~~a third doped region formed in the substrate,~~ wherein the third doped region ~~is~~ comprises a contact to the first well;

~~a fourth doped region formed in the second well; and~~

~~a fifth doped region formed in the substrate,~~ wherein the fifth doped region ~~is~~ comprises a contact to the third well, and

wherein the first and second doped regions are connectable to a contact pad ~~for an ESD in an ESD event~~, the third and fifth doped regions are connectable to a power supply, ~~and~~ the fourth doped region is connectable to an ESD detection circuit, ~~wherein~~ and the ESD detection circuit is coupled to the contact pad ~~for detecting the ESD~~.

Claim 28. (Cancelled).

29. (Currently Amended) The semiconductor device of claim 27, wherein the ESD detection circuit ~~triggers~~ is adapted to trigger the first and second BJTs to conduct ~~the ESD~~ current from the first and second doped regions to the third and fifth doped regions, respectively, or from the third and fifth regions to the first and second doped regions, respectively.

30. (Original) The semiconductor device of claim 27, wherein the first doped region, the second doped region, the third doped region, the fourth doped region, and the fifth doped region are isolated from each other by a plurality of gate structures, wherein a first gate structure is formed between the first and third doped regions, and the first gate structure, the first doped region, the third doped region, and the second well form a first MOS transistor, wherein a second gate structure is formed between the second and fifth doped regions, and the second gate structure, the second doped region, the fifth doped region, and the second well form a second MOS transistor.

31. (Currently Amended) The semiconductor device of claim 30, wherein the first gate and the second gate are both connectable to the ESD detection circuit to trigger the first and second BJTs to discharge ~~the ESD~~ current in an ESD event.

Claims 32-36 (Cancelled).

37. (Currently Amended) The semiconductor device of claim 2, wherein the deep well ~~is~~ comprises an n-type well.

38. (Previously Presented) The semiconductor device of claim 1, wherein the deep well further physically isolates the substrate from the first well.

39. (Currently Amended) The semiconductor device of claim 26. wherein the deep well ~~is~~ comprises an n-type well.

40. (New) An apparatus, comprising:

a first well formed in a semiconductor substrate;

a second well formed in the substrate adjacent to the first well, the second well of a different conductivity type than the first well;

a deep well formed in the substrate and physically isolating at least the first well from the substrate;

first and second doped regions formed at least partially in the first well and of the same conductivity type as the first well; and

a third doped region formed in the first well between the first and second doped regions, the third doped region of a different conductivity type than the first well,

wherein the first doped region is formed in both the first well and the second well, and

wherein the first doped region is adapted to receive a trigger current and/or a trigger voltage.

41. (New) The apparatus of claim 40, wherein the first well comprises an p-well, the second well comprises a n-well, the deep well comprises an n-well, and the first doped region comprises an p-type doped region.

42. (New) The apparatus of claim 41, further comprising:

a third well formed in the substrate adjacent to the first well and spaced apart from the second well, the third well of a same conductivity type as the second well, and

wherein the second doped region is formed in both the first well and the third well.

43. (New) The apparatus of claim 40, wherein the deep well further physically isolates the substrate from the first well.

44. (New) The apparatus of claim 40, further comprising:

an electrostatic discharge (ESD) detection circuit coupled to the first doped region.

45. (New) The apparatus of claim 40, wherein the first well comprises an n-well, the second well comprises a p-well, the deep well comprises an n-well, and the first doped region comprises an n-type doped region.

46. (New) The apparatus of claim 40, further comprising:

a plurality of isolation regions adapted to electrically isolate the first, second, and third doped regions from each other.

47. (New) The apparatus of claim 46, wherein the isolation regions comprise shallow trench isolations (STIs).

48. (New) The apparatus of claim 46, wherein the isolation regions comprise oxidation of silicon (LOGOS) regions.

49. (New) The apparatus of claim 46, wherein the isolation regions comprise dummy gate structures.

50. (New) The apparatus of claim 40,

wherein the first well, the second well, and the third doped region comprise, respectively, a collector, a base, and an emitter of a parasitic bipolar junction transistor (BJT), and

wherein the parasitic BJT is adapted to discharge an electrostatic discharge (ESD) current in response to the trigger current or the trigger voltage.